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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/665,415	09/20/2000	Kazuyuki Nakagawa	500-0-240	8537

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EXAMINER	
PAREKH, NITIN	
ART UNIT	PAPER NUMBER
2811	

DATE MAILED: 04/07/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/665,415	Applicant(s) NAKAGAWA ET AL.	
	Examiner Nitin Parekh	Art Unit 2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 January 2003* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-4* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-4* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *20 September 2000* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *6 & 9* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Request for Continued Examination

1. A request for continued examination (RCE) under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 01/24/03 has been entered. An action on the RCE follows.

2. The amendment filed on 12-23-02 has been entered.

Information Disclosure Statement

3. The Information Disclosure Statement filed on 09-30-02 has been considered.

Claim Objections

4. Claim 4 is objected to because of the following informalities:

Claim 4, line 2: Delete "radically" and insert — "radially" —.

Appropriate correction is required.

Claim Rejections - 35 USC § 103

5. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 1, 3 and 4 are rejected under 35 U.S.C. 103(a) as being unpatentable over Jiang et al. (US Pat. 6455354).

Regarding claim 1, Jiang et al. disclose a semiconductor device comprising:

- a semiconductor element having a primary surface (112 in Fig. 6) with an element electrode (112 and 134 respectively in Fig. 6) and a back surface
- a circuit board/printed circuit board (PCB) having a primary surface (114 in Fig. 6) and a back surface with a board electrode (138 in Fig. 6), the circuit board having a predetermined opening hole (106 in Fig. 6)
- the primary surface of the element being bonded to the primary surface of the circuit board by means of an adhesive layer (108 in an embodiment as shown in

- Fig. 6), the adhesive layer being of the same size/width as that of the semiconductor element and smaller than that of the PCB
- the element electrode of the semiconductor element being connected to the board electrode provided on the back surface of the board via the opening hole
- the surrounding regions of the side surfaces and back surface of the semiconductor element on the circuit board being sealed with an encapsulate/resin to assume a tapered profile/structure (146 in Fig. 6), and
- the semiconductor element and the PCB directly contacting each other via the adhesive layer in order to provide increased contact area to relieve stress/tension between the semiconductor element and the PCB and to reduce flexing/twisting of the assembly and the encapsulation defects (Col. 5, line 35-45; Col. 8, line 22-27).

(Fig. 6; Fig. 1-6; Col. 7, line 50- Col. 8, line 60).

Jiang et al. fail to teach the adhesive layer in the embodiment of Fig. 6 being extended outside an outer edge of the primary surface of the semiconductor element without reaching that of the circuit board.

Jiang et al. further teach (see an embodiment shown in Fig. 10) selecting a size and a configuration of the adhesive layer where the adhesive layer extends beyond the outer edge/edges of the semiconductor element (see 108 in Fig. 10 being extended in

width direction only) without reaching that of the circuit board so that the visual inspection capability can be enhanced and the encapsulation defects at the edges/corners of the semiconductor element can be reduced for the device (Col. 9, line 5-12; Col. 7-9).

It would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate an adhesive layer extending outside the outer edges of the primary surface of the semiconductor element in length/width direction, radially and completely around without reaching that of the circuit board so that the stress/tension between the semiconductor element and the PCB, the flexing/twisting of the assembly and the encapsulation defects can be reduced and adhesion and rigidity can be improved in Jiang et al's device.

Regarding claim 3, Jiang et al. teach substantially the entire claimed structure as applied to claim 1, above including the surrounding regions of the side surfaces and back surface of the semiconductor element being sealed with the resin.

Regarding claim 4, Jiang et al. teach substantially the entire claimed structure as applied to claim 1, above including the adhesive layer extending radially outward and completely around the primary surface of the semiconductor element.

7. Claim 2 is rejected under 35 U.S.C. 103(a) as being unpatentable over Jiang et al. (US Pat. 6455354) in view of Taguchi et al. (US Pat. 6429372).

Regarding claim 2, Jiang et al. teach substantially the entire claimed structure as applied to claim 1, except the surrounding regions of the sealed resin to assume a flange structure.

Taguchi et al. teach using the sealing resin having surrounding regions (21 in Fig. 2) of the side surfaces of the semiconductor element on the circuit board being sealed with a resin to assume a chamfered flange structure to improve rigidity and stiffness for a device (Col. 10, line 10-48).

It would have been obvious to a person of ordinary skill in the art at the time invention was made to incorporate the surrounding regions of the sealed resin to assume a flange structure as taught by Taguchi et al. so that the stress/tension between the semiconductor element and the PCB, the flexing/twisting of the assembly and the encapsulation defects can be reduced and rigidity can be improved in Jiang et al's device.

Response to Arguments

8. Applicant's arguments with respect to claims 1-4 have been considered but are moot in view of the new ground(s) of rejection.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nitin Parekh whose telephone number is 703-305-3410. The examiner can normally be reached on 09:00AM-05:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tom Thomas can be reached on 703-308-2772. The fax phone numbers for the organization where this application or proceeding is assigned are 703-308-7722, 703-308-7724 or 703-872-9318 (Right FAX) for regular communications; 703-872-9310 (Right FAX) for After Final communications and 703-872-9310 (Right FAX) for customer service.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-306-3431.

Tom Thomas

Nitin Parekh

03-30-03

TOM THOMAS
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800